Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. The following listing provides the amended claims with the amendments marked with deleted material ~~struck through~~ and new material underlined to show the changes made.

Listing of Claims:

Claims 1-15 (Previously cancelled)

16. (Twice Amended) An integrated circuit comprising:

a plurality of metal layers comprising a plurality of conductors to interconnect components in said integrated circuit, said metal layers comprising:

a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposed in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors and said self contained layout section comprising a routing of conductors developed independent from routing of conductors for circuits outside said self contained layout section in said integrated circuit; and

a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of the metal layer directly adjacent to said portion of said metal layer for said self contained layout section, and wherein conductors for said second metal layer group are routed independent from routing of conductors for said self contained layout section,

whereby said preferred Manhattan direction conductors of said self contained layer within said first metal group do not electrically cross-couple with conductors of said second metal layer

group regardless of whether said self contained layout conductors are deposed in either a horizontal or vertical direction.

17. (Original) The integrated circuit as set forth in claim 16, wherein said self contained layout section is independent of a layout for said second metal layer group.

18. (Original) The integrated circuit as set forth in claim 16, further comprising a plurality of self contained layout sections in said first metal layer.

19. (Original) The integrated circuit as set forth in claim 18, wherein at least one of said self contained layout sections comprise a wiring direction perpendicular to a wiring direction of a second one of said self contained layout sections.

20. (Original) The integrated circuit as set forth in claim 16, wherein said self contained layout section comprises an entire one of said metal layer in said first metal layer group.

21. (Original) The integrated circuit as set forth in claim 16, wherein said first metal layer group comprises three metal layers.

22. (Original) The integrated circuit as set forth in claim 21, wherein said three metal layers each comprise conductors deposed in preferred Manhattan directions, wherein:

said first metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said second metal layer; and

said second metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said third metal layer.

23. (Original) The integrated circuit as set forth in claim 16, wherein said diagonal direction comprises a direction 45 degrees relative to said integrated circuit boundaries.

24. (Original) The integrated circuit as set forth in claim 16, wherein said diagonal direction comprises a direction 60 degrees relative to said integrated circuit boundaries.

25. (Original) The integrated circuit as set forth in claim 16, wherein said self contained layout comprises a layout for a memory block.

Claim 26 (canceled)

27. (Original) The integrated circuit as set forth in claim 16, wherein said self contained layout section comprises a section less than 10 percent of the entire area of said metal layer.

28. (Twice Amended) A method for deposing a plurality of metal layers comprising a plurality of conductors to interconnect components of an integrated circuit, said method comprising the steps of:

designating a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposed in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors and said self contained layout section comprising a routing of conductors, for the portion of said metal layer, developed independent from routing of conductors for circuits outside said self contained layout section in said integrated circuit; and

designating a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred

diagonal direction in a portion of the metal layer directly adjacent to said portion of said metal layer for said self contained layout, and wherein conductors for said second metal layer group are routed independent from routing of conductors for said self contained layout section,

whereby said preferred Manhattan direction conductors of said self contained layer within said first metal group do not electrically cross-couple with conductors of said second metal layer group regardless of whether said self contained layout conductors are deposed in either a horizontal or vertical direction.

29. (Original) The method as set forth in claim 28, wherein said self contained layout section is independent of a layout for said second metal layer group.

30. (Original) The method as set forth in claim 28, further comprising a plurality of self contained layout sections in said first metal layer.

31. (Original) The method as set forth in claim 30, wherein at least one of said self contained layout sections comprise a wiring direction perpendicular to a wiring direction of a second one of said self contained layout sections.

32. (Original) The method as set forth in claim 28, wherein said self contained layout section comprises an entire one of said metal layer in said first metal layer group.

33. (Original) The method as set forth in claim 28, wherein said first metal layer group comprises three metal layers.

34. (Original) The method as set forth in claim 33, wherein said three metal layers each comprise conductors deposed in preferred Manhattan directions, wherein:

said first metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said second metal layer; and

said second metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said third metal layer.

35. (Original) The method as set forth in claim 28, wherein said diagonal direction comprises a direction 45 degrees relative to said integrated circuit boundaries.

36. (Original) The method as set forth in claim 28, wherein said diagonal direction comprises a direction 60 degrees relative to said integrated circuit boundaries.

37. (Original) The method as set forth in claim 28, wherein said self contained layout comprises a layout for a memory block.

Claim 38 (canceled)

39. (Original) The method as set forth in claim 28, wherein said self contained layout section comprises a section less than 10 percent of the entire area of said metal layer.

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